U.S. Patent Application

of

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relating to

MULTIPLEXING AND DEMULTIPLEXING METHOD AND APPARATUS

Express Mail No. EV 005523503 US

MULTIPLEXING AND DEMULTIPLEXING METHOD AND APPARATUS

CROSS-REFERENCE TO RELATED APPLICATION

This application is a continuation of International Application PCT/EP99/04215 having an international filing date of June 17, 1999 and from which priority is claimed under all applicable sections of Title 35 of the United States Code including, but not limited to, Sections 120, 363 and 365 (c).

FIELD OF THE INVENTION

The present invention relates to a multiplexing and demultiplexing method and apparatus to be used in a data network such as an ATM (Asynchronous Transfer Mode) network.

BACKGROUND OF THE INVENTION

ATM is a transfer mode in which information is organized into cells. It is asynchronous in the sense that the recurrence of cells containing information from an individual user is not necessarily periodic. ATM is a layered architecture allowing multiple services like voice, data and video to be mixed over the network.

It is desirable that a common interface between the lowest physical layer (PHY) and upper layer modules such as the ATM layer is defined, to thereby allow a common PHY interface in ATM subsystems across a wide range of speeds and media types.

In many cases, an arrangement is provided, where a plurality of PHY devices are connected via the PHY

interface to a single ATM device. Thus, an address has to be allocated to the PHY devices, which is used by the higher layer device in order to individually access one of the PHY devices in order to perform a data transfer. However, the number of available addresses according to the PHY interface specification may not be large enough to support a desired number of physical devices.

Although conversion circuits such as multiplexer/demultiplexer (MUX/DEMUX) circuits are known to connect a plurality of non-addressable PHY devices to a higher layer device, these circuits are not suitable for overcoming the above problem, because they also demand a respective address for each of the non-addressable PHY devices.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention, to provide a multiplexing and demultiplexing method and apparatus, by means of which the number of PHY devices connectable via a PHY interface can be increased without increasing the required number of addresses.

This object is achieved by a multiplexing method for supplying input data received from one of a plurality of input channels to an output channel, comprising the steps of:
providing a plurality of input buffers respectively connected to the plurality of input channels, and an output buffer connected to the output channel;
storing the received input data in a respective one of the plurality of input buffers; and
releasing transmission of the input data from the respective one of the plurality of input buffers to the

interface to a single ATM device. Thus, an address has to be allocated to the PHY devices, which is used by the higher layer device in order to individually access one of the PHY devices in order to perform a data transfer. However, the number of available addresses according to the PHY interface specification may not be large enough to support a desired number of physical devices.

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storing the received input data in a respective one of the plurality of input buffers; and

releasing transmission of the input data from the respective one of the plurality of input buffers to the

output buffer, when the output buffer is capable of receiving data.

Furthermore, the above object is achieved by a demultiplexing method for supplying input data received from an input channel to a plurality of output channels, comprising the steps of:

providing an input buffer connected to the input channel and a plurality of output buffers respectively connected to the plurality of output channels;

storing the input data in the input buffer; and

releasing transmission of the input data from the input buffer to the plurality of output buffers, when all of the plurality of output buffers are capable of receiving data.

Additionally, the above object is achieved by a multiplexing apparatus for supplying input data received from one of a plurality of input channels of the multiplexing apparatus to an output channel thereof, comprising:

a plurality of input buffer means respectively connected to the plurality of input channels, wherein the input data is stored in a respective one of the plurality of input buffer means;

output buffer means connected to the output channel; and

control means for releasing a transmission from the respective one of the plurality of input buffer means to the output buffer means, when the output buffer means is capable of receiving data.

Moreover, the above object is achieved by a demultiplexing apparatus for supplying input data received from an input channel of the demultiplexing apparatus to a plurality of output channels thereof, comprising:

input buffer means for storing the input data;

a plurality of output buffer means respectively connected to the plurality of output channels; and
control means for releasing a transmission from the input buffer means to the plurality of output buffer means, when all of the plurality of output buffer means are capable of receiving data.

Accordingly, all physical devices can be placed behind a single interface address and receive the same data. Then, the PHY devices may decide themselves whether the received data belongs to them or not. In one direction (demultiplexing), the data is broadcasted to all PHY devices, while, in the other direction (multiplexing), one PHY device may individually transmit its data at a time.

Accordingly, no further interface addresses are required for the PHY devices connected via a multiplexer/demultiplexer according to the present invention.

Preferably, the input and output buffers can be First-In-First-Out (FIFO) buffers, so that a plurality of data packets can be received and their order maintained.

The plurality of input channels can be connected to a plurality of PHY devices having the same interface address allocated. Thus, even the number of addresses of the PHY devices as such can be reduced, since they are connected to the upper layer network via the multiplexer/demultiplexer according to the present invention, which does not require any addresses for performing the multiplexing/demultiplexing operation.

In particular, the PHY devices may be UTOPIA (Universal Test & Operations PHY Interface for ATM) level 1 compliant. Thus, the multiplexer/demultiplexer according to the

present invention can be used as a converter between a UTOPIA Layer 1 interface and a UTOPIA Layer 2 interface, such that non-addressable Layer 1 PHY devices can be connected to an Layer 2 device. In this case, the output channel may be connected to an ATM device compliant to the UTOPIA level 1 or level 2 interface specifications.

BRIEF DESCRIPTION OF THE DRAWINGS

In the following the present invention will be described in greater detail on the basis of a preferred embodiment with reference to the accompanying drawings, in which:

Fig. 1 is a principle block diagram of a basic ATM reference model,

Figs. 2A and 2B are respectively a block diagram of a UTOPIA level 1 reference configuration and a UTOPIA level 2 reference configuration,

Fig. 3 is a block diagram of a multiplexer/demultiplexer according to the preferred embodiment of the present invention, and

Figs. 4A and 4B are respectively a flow diagram of a control operation of a transmit interface and of a receive interface, according to the preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following, the preferred embodiment of the multiplexing and demultiplexing method and apparatus according to the present invention will be described on the basis of a UTOPIA interface for an ATM system.

The UTOPIA data path interface defines an interface between the physical layer (PHY) and upper layer modules such as the ATM layer and the corresponding management entities (such as a microprocessor or the like). In practice, the UTOPIA data path interface may, however, as well be used between two circuits which both belong to the ATM layer (i.e. ATM to ATM). In particular, the UTOPIA data path specification defines two interface signal groups i.e. transmit (Tx) and receive (Rx).

Fig. 1 shows a basic ATM reference model comprising the UTOPIA interface. According to Fig. 1, three lower level layers are defined to implement the features of ATM. An ATM adaptation layer (AAL) 3 assures appropriate service characteristics and divides all types of data received from higher layers 4 into an 48 byte payload that will make up an ATM cell. Furthermore, an ATM adaptation layer 3 adds a 5 byte header information to the data to be transmitted, so as to assure that the ATM cell is transmitted on the right connection. A physical layer (PHY) 1 defines the electrical characteristics and network interfaces i.e. how the bits are transmitted via the wire. The above defined layers are controlled by a management & control function 5.

As shown in Fig. 1, the UTOPIA interface defines a standard interface between the ATM layer 2 and the PHY layer 1 of ATM subsystems. The interface part where data flows from the ATM layer 2 to the PHY layer 1 is labeled Transmit Interface, and the interface part where data flows from the PHY layer to the ATM layer is labeled Receive Interface.

Transmit and receive transfers are synchronized via the respective interface transfer clock. With an 8-bit data path and a maximum clock rate of 25 MHz, this interface

supports rates from sub-100 to 155 Mbps. Furthermore, higher rates (e.g. 622 Mbps) may be supported by extending the data path to 16 bits and using a faster transfer clock.

The transfer of data is synchronized at the cell level via a Start Of Cell (SOC) signal. This signal is asserted when the data transfer path contains the first byte of a cell.

Given that the PHY layer 1 must accept transfer synchronizing clocks from the ATM layer 2, the PHY layer 1 will require rate matching buffers such as FIFOs. With the use of such FIFOs, flow control signals can be provided to allow both the ATM layer 2 and the PHY layer 1 to throttle the transfer rate.

The Receive Interface transfers data only when ATM layer 1 requests it by asserting an Enable signal. The interface also provides an Empty/Cell Available signal from the PHY layer 1 to allow a PHY layer rate control. A false Empty signal indicates a valid received octet and provides an octet-level flow control. A true Cell Available signal indicates the availability of a whole cell and provides a cell-level flow control.

The Transmit Interface transfers data only when the ATM layer 2 requests it by asserting an Enable signal. The interface also provides a Full/Cell Available signal from the PHY layer 1 to allow a PHY layer rate control. The Full signal is asserted if more than four additional bytes would cause a PHY buffer overflow. The Available signal indicates that enough space is left in the transmit FIFO to hold a complete cell.

In particular, the UTOPIA interface specification is divided into a Level 1 specification and a Level 2

specification. The UTOPIA Level 1 reference configuration is shown in Fig. 2A. According to the Level 1 reference configuration, one ATM device 20 is connected to one PHY device 10. Accordingly, the Level 1 specification specifies an 8 bit wide data path using an octet-level or a cell-level handshake, operating up to 25 MHz with a single PHY device, a cell format and extra signals for a 16-bit wide data path for future use.

Fig. 2B shows a Level 2 reference configuration, wherein an ATM device 21 is connected to a plurality of PHY devices 11 to 1n, wherein n < 8 for ATM layers 2 intended for 455 Mbps, and n < 4 for ATM layers 2 intended for 622 Mbps. The virtual space is set up for n < 31. According to Fig. 2B, addresses 1 to n are allocated by the management & control function 5 shown in Fig. 1.

In the following, the operation of the Transmit Interface, i.e. ATM → PHY, is briefly described.

In Level 1 UTOPIA, there is only one PHY device 10 and the control signal Empty/Cell Available is utilized to convey the transfer status to the ATM device 20. In Level 2 UTOPIA, only one of the PHY devices 11 to 1n at a time can be selected for a cell transfer. The ATM device 21 selects a PHY device by using a corresponding address. Once a PHY device is selected, the data transfer is accomplished by a handshake processing.

If a Level 2 PHY device is to be operated in a Level 1 PHY environment, the address of the Level 2 PHY device is set to a value programmed by the management & control function 5.

In the following, the Receive Interface is described.

In Level 1 UTOPIA, the signal Full/Cell Available is used to convey a transfer status to the ATM device 20. In Level 2 UTOPIA, only one of the PHY devices 11 to 1 n at a time is selected for a cell transfer. The ATM device 21 selects the PHY device by using the corresponding address. Once a PHY device is selected, the data transfer is accomplished by the handshake processing.

According to the preferred embodiment of the present invention, a UTOPIA multiplexer/demultiplexer and a method thereof is defined, to which a plurality of PHY devices can be connected via a UTOPIA Layer 1 interface and which can be connected to an ATM device via a UTOPIA Layer 1 or Layer 2 interface. Thus, a plurality of PHY devices can be connected to an ATM device by using a single address.

Fig. 3 shows a principle block diagram of the UTOPIA multiplexer/demultiplexer 300 according to the preferred embodiment of the present invention.

According to Fig. 3, the multiplexer/demultiplexer 300 comprises e.g. four FIFO buffers 311 to 314 at the PHY layer side. The PHY FIFO buffers 311 to 314 are respectively connected to Layer 1 PHY devices 101 to 104 via a UTOPIA Layer 1 interface. Furthermore, the multiplexer/demultiplexer 300 comprises a FIFO buffer 301 at the ATM layer side. The ATM FIFO 301 is connected to an ATM device 200 via a UTOPIA Layer 1 or Layer 2 interface.

However, it is to be noted that more or less than the above four PHY devices 101 to 104 and corresponding FIFO buffers 311 to 314 could be connected via the multiplexer/demultiplexer 300 to the ATM device 200, as well. Furthermore, if a Layer 1 interface is used, only one multiplexer/demulti-

plexer 300 can be connected to the ATM device 200. However, if a Layer 2 interface is provided, a plurality of multi-plexers/demultiplexers 300 can be connected to a single ATM device 200 by allocating corresponding addresses to the multiplexers/demultiplexers 300.

Furthermore, the multiplexer/demultiplexer 300 comprises a control logic 320 arranged to exchange control signals with the FIFO buffers 301 and 311 to 314, to thereby control the multiplexing/demultiplexing operation.

In the following, the operation of the multiplexer/demultiplexer 300 is described with reference to Figs. 4A and 4B.

Fig. 4A shows a principle flow diagram of the demultiplexing processing, i.e. UTOPIA Transmit Interface function, performed by the control logic 320.

In case the ATM device 200 transmits an ATM cell or a data octet to one of the PHY devices 101 to 104, a Layer 1 or Layer 2 Transmit Interface data transfer to the ATM FIFO 301 is performed, as described above. The control logic 320 determines in step S100 whether data is available at the ATM FIFO 301. If not, step S100 is repeated until the control logic 320 receives a corresponding control signal from the ATM FIFO 301. Having received the transmitted data, the ATM FIFO 301 transmits a corresponding control signal to the control logic 320, and the processing of the control logic 320 moves to step S101 so as to determine whether all of the PHY FIFOs 311 to 314 have signalized their capability of receiving data, i.e. availability of empty buffer capacity. If not, step S101 is repeated until the control logic 320 receives a corresponding indication from all PHY FIFOs 311 to 314.

If enough buffer capacity is available at all PHY FIFOs 311 to 314, the control logic 320 issues a release signal to the ATM FIFO 301 to thereby release a transmission operation of the received data via an internal bus system to all of the PHY FIFOs 311 to 314 (step S102). In this respect, it is to be noted, that the internal bus interface between the ATM FIFO 301 and the PHY FIFOs 311 to 314 can be a usual FIFO interface or a UTOPIA Layer 1 interface with the corresponding processings.

Having received the transmitted data, the PHY FIFOs 311 to 314 perform a usual Layer 1 Transmit Interface data transfer to the PHY devices 101 to 104. The PHY devices 101 to 104 may then decide whether the data belongs to them, based on a corresponding information which may be provided in the UTOPIA cell format.

Thus, in the above described egress direction (ATM → PHY), the control logic 320 waits until all PHY FIFO buffers 311 to 314 can receive data, and then releases the ATM FIFO buffer 301 connected to the ATM device 200 to transmit data.

In the following, the multiplexing function i.e. Receive Interface data transfer, of the multiplexer/demultiplexer 300 according to the preferred embodiment is described with reference to Fig. 4B.

If one of the PHY devices 101 to 104 wishes to transmit an ATM cell or data octet to the ATM device 200, it performs a usual UTOPIA Receive Interface data transfer to the corresponding PHY FIFO via the UTOPIA Layer 1 interface.

Then, the control logic 320 waits in step S200 until the availability of the transmitted data at one of the PHY

FIFOs 311 to 314 is signalized by a corresponding control signal. If so, the control logic 320 waits in step S201 until it has received a control signal from the ATM FIFO 301, which indicates that the ATM FIFO 301 is capable of receiving data, i.e. enough buffer capacity is available.

If the ATM FIFO 301 has indicated its capability of receiving data by a corresponding control signal, the control logic 320 issues in step S202 a released signal to the requesting PHY FIFO in order to release a data transmission from the respected one of the PHY FIFOs 311 to 314 to the ATM FIFO 301 via the internal bus system. Having received the transmitted data, the ATM FIFO 301 performs a usual UTOPIA Receive Interface data transfer to the ATM device 200 via the UTOPIA Layer 1 or Layer 2 interface, as described above.

Accordingly, in the above described ingress direction (PHY → ATM), the control logic 320 releases one of the PHY FIFO buffers 311 to 314 to transmit data, if the receiving ATM FIFO 301 is able to receive data. Thus, no data collisions will occur on the internal bus system.

It is to be noted that the above described multiplexer/de-multiplexer 300 can be applied to any data network where an interface is to be established between a plurality of physical layer or higher layer devices and a higher layer device, to thereby reduce the number of required device addresses. In particular, the multiplexer/demultiplexer 300 according to the preferred embodiment may as well be used for connecting the ATM device 200 to a plurality of other ATM devices which may be UTOPIA level 1 or level 2 compliant. The control logic may be a hardware arrangement or a microprocessor controlled on the basis of a corresponding software program.

In summary, a multiplexing and demultiplexing method and apparatus are described, wherein a transmission of input data from one or a plurality of input buffers to a plurality of or one output buffer, respectively, is released when all of the plurality of or the one output buffer is capable of receiving data. Thus, a plurality of devices can be connected to another device using only one address. The plurality of devices may then decide themselves whether the data belongs to them or not. In one direction, the data is broadcasted to all of the plurality of devices and, in the other direction, one of the plurality of devices can transmit data at a time. Accordingly, interface addresses can be saved in case the number of addresses is not enough for all of the plurality of devices.

The above description of the preferred embodiment and the accompanying drawings are only intended to illustrate the present invention. The preferred embodiment of the invention may vary within the scope of the attached claims.